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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2112	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,427	BORMANN ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 9-17, 19-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arends et al. (US Patent 6,560,712) in view of Hannah (US Patent 5,784,581)

As per claims 1,14, Arends discloses an apparatus comprising:

A configurable link which couples a computer's central processing unit (CPU) to a bus as a default bus master and couples a first peripheral device to the bus as a slave device if the computer's CPU is in a first power management state; and (col.4, lines 17-61) wherein normal mode implies first power state and bus arbitration implies configurable link)

Arends discloses all the limitations as above except couples the first peripheral device to the bus as the default bus master if the computer's CPU is in a second power management state. However, Hanna discloses for the operating a peripheral device as either a master or slave and permitting the device to communicate with other devices directly even though the host is inactive or without requiring an active host

(col.2, lines 1-24), this inherently discloses when CPU is in second power management state, peripheral device becomes the default bus master.

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Hanna's teaching into Arend's system so as to detect the CPU for better performance.

As per claim 2, Arends discloses wherein the first power management state and the second power management state each comprises a set of power management states. (col.4, lines 17-61)

As per claim 3, Arends discloses wherein the first peripheral device is capable of operating as a conventional peripheral device when coupled to the bus as the slave device. (col.2, lines 50-63)

As per claims 4, 15, 20 Arends discloses all the limitations as above except wherein the first peripheral device is capable of operating as the default bus master for the computer without assistance from the CPU. However, Hanna discloses for the operating a peripheral device as either a master or slave and permitting the device to communicate with other devices directly even though the host is inactive or without requiring an active host (col.2, lines 1-24)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Hanna's teaching into Arend's method so as to detect the CPU for better performance.

As per claims 5, 19, Arends discloses all the limitations as above except wherein the first peripheral device causes the configurable link to couple the first

peripheral device to the bus as the default bus master when the CPU is in a second power management state. However, Hanna discloses for the operating a peripheral device as either a master or slave and permitting the device to communicate with other devices directly even though the host is inactive or without requiring an active host (col.2, lines 1-24), this inherently discloses when CPU is in second power management state, peripheral device becomes the default bus master.

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Hanna's teaching into Arend's system so as to detect the CPU for better performance.

As per claims 6, 17, Arends discloses wherein the second power management state the computer's CPU is in a sleeping state. (col.3, line 28-col.4, line 61) wherein low power mode implies sleeping state)

As per claim 9, Arends discloses the apparatus further comprising an input/output hub communicatively coupling the configurable link and the central processing unit (CPU). (col.2, lines 50-63, since arbiter is providing, configured signals to enable data and address outputs, it is inherent that it arbiter performs as input/output hub)

As per claim 10, Arends discloses wherein the first level of access, the CPU manages the input/output hub to control communications to and from the first peripheral device when the computer's CPU is the default bus master. (col.3, line 28-col.4, line 38)

As per claim 11, Arends discloses all the limitations as above except wherein the configurable link enables the first peripheral device to manage the input/output hub to control communications to and from the first peripheral device when the first peripheral device is the default bus master. However, Hanna discloses for the operating a peripheral device as either a master or slave and permitting the device to communicate with other devices directly even though the host is inactive or without requiring an active host (col.2, lines 1-24), this inherently discloses when CPU is in second power management state, peripheral device becomes the default bus master.

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Hanna's teaching into Arend's system so as to detect the CPU for better performance.

As per claim 12, Arends discloses the apparatus further comprising a second peripheral device communicatively coupled to the input/output hub. (col.2, lines 50-63)

As per claims 13, 24 Arends discloses all the limitations as above except the first peripheral device can communicate directly with the second peripheral device without assistance from the CPU. However, Hanna discloses for the operating a peripheral device as either a master or slave and permitting the device to communicate with other devices directly even though the host is inactive or without requiring an active host (col.2, lines 1-24)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Hanna's teaching into Arend's method so as to detect the CPU for better performance.

As per claim 21, dislcoses a system comprising:

- A sub-system to detect the power management state of a central processor; (col.3, line 28-col.4, line 38)
- A sub-system to determine whether the central processor is in a first power management state or a second power management state; (col.4, lines 33-41), wherein normal and low power mode imply 1st and 2nd state)
- A sub-system to couple the central processor to a bus as a default bus master and to couple a first peripheral device to the bus as a slave device if the central processor is in a first power management state; and (col.3, line 28-col.4,line 41)

Arends discloses all the limitations as above except A sub-system to couple the first peripheral device to the bus as the default bus master if the central processor is in a second power management state. However, Hanna discloses for the operating a peripheral device as either a master or slave and permitting the device to communicate with other devices directly even though the host is inactive or without requiring an active host (col.2, lines 1-24), this inherently implies when CPU is in second power management state, peripheral device becomes the default bus master.

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Hanna's teaching into Arend's system so as to detect the CPU for better performance.

As per claim 22, Arends discloses all the limitations as above except the system further comprising a sub-system to initiate a data transfer from the first peripheral device if the central processor is in the second power management state. However, Hanna discloses for the operating a peripheral device as either a master or slave and permitting the device to communicate with other devices directly even though the host is inactive or without requiring an active host (col.2, lines 1-24), this inherently implies when CPU is in second power management state, peripheral device initiate a data transfer.

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Hanna's teaching into Arend's system so as to detect the CPU for better performance.

As per claim 23, Arends discloses all the limitations as above except the system further comprising a sub-system to buffer data at the first peripheral device if the central processor is in the second power management state. However, Hanna discloses for the operating a peripheral device as either a master or slave and permitting the device to communicate with other devices directly even though the host is inactive or without requiring an active host (col.2, lines 1-24), this inherently implies when CPU is in second power management state, peripheral

device becomes the default bus master and initiate a data transfer to/from peripheral device.

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Hanna's teaching into Arend's system so as to detect the CPU for better performance.

As per claim 25, Arends discloses the system further comprising a sub-system to delay the central processor from transitioning from the second power management state to the first power management state. (col.3, lines 9-12), wherein a minimal delay due to reinitiating implies delay the transitioning from 2nd power state to 1st power state. (col.4, lines 35-61)

3. Claims 7, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arends et al. (US Patent 6,560,712) in view of Hannah (US Patent 5,784,581) and further in view of Odaohhara et al. (US Patent 6,574,740)

Arends discloses all the limitations as above except wherein the second power management state includes power modes s3-s5 as defined in the Advanced Configuration and Power Interface (ACPI) specification. However, Odaohhara discloses ACPI that forms a portion of the OS and upon the detection of the interrupt signal from power controller and passes to ASL to change operation mode of CPU. (col.13, lines 6-47)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Odaohhara's teaching into Arend's method so have the same purposes of controlling power consumption of CPU.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arends et al. (US Patent 6,560,712) in view of Hannah (US Patent 5,784,581) and further in view of Shinoda (JP Patent 406337743A)

Arends discloses all the limitations as above except wherein the transfer rate over the configurable link when the first peripheral device is the default bus master is different than when the computer's CPU is the default bus master. However, Shinoda discloses input device has a main CPU 1 which controls the basic constitution of a computer and a sub-CPU 2 which is controlled by the main CPU 1 and places the main CPU 1 in a sleep state while the sub-CPU2 operates. However, a data communication is fast transfer rate. See abstract

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Shinoda's teaching into Arends's system so as to reduce the power consumption.

Response to Amendment

5. Applicant's amendment filed on 2/10/04 have been fully considered but are not place application in condition for allowance.

In response to applicant's argument that Arends a peripheral device becomes the default bus master when a processor that is the CPU enters a low power mode. As Hanna notes at (col.2, lines 1-24) discloses for the operating a peripheral device as either a master or slave and permitting the device to communicate with other devices directly even though the host is inactive or without requiring an active host, this inherently discloses when CPU is in second power management state, peripheral

device becomes the default bus master and operate while CPU is inactive. Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

Notice to Applicant(s)

6. The examiner refers to Shinoda (JP Patent 406337743A) reference as a prior art for the claim 8 rejection in the instant Office Action, and it is referred to the original copy of foreign reference in foreign language(i.e., Japanese). The Examiner attaches a machine translated copy of the reference for the convenience of the Applicant. However, the Examiner cautions the Applicant that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

April 7, 2004

Khanh Dang
Primary Examiner